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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,846	02/25/2004	Qiang Luo	50019.0272US01	2949

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,846	LUO, QIANG	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/1/04;8/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-7, in the reply filed on 10/7/05 is acknowledged. The Examiner notes the Applicant's cancellation of non-elected claims 8-18.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, the extent of the claimed depletion region depends greatly on the specific bias voltage applied to the junction. Thus, it is unclear at what ranges of bias voltages the depletion region must not extend to the first oxide layer in order to meet the limitations of the claim, and likewise, it is unclear exactly how long the interval between the oxide layer and the diode electrode structure must be.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2001/0017382 to Rhodes et al. (cited by applicant).

Regarding claim 1, Rhodes discloses a method for low dark current imaging, comprising: forming a first well (112, 212) of a first polarity type (p-type; paragraph 0025); forming a first oxide layer (120, 220) on the surface of the first well (see figure 7) such that the first oxide layer comprises an opening through which a portion of the first well is exposed (region between the two field oxide portions; see figures 4 and 7); and forming a diode electrode structure (110 and 130; alternately 230; see figures 6 and 9) of a second polarity type opposite the first polarity type (n-type; paragraphs 0026, 0028; 0043), wherein the diode electrode structure is formed within an area within the exposed portion of the first well (see figures 6 and 9) such that an intervening portion of the first well exists between the diode electrode structure and first oxide layer (see figures 6 and 9; intervening portion is the portion of 112/212 exposed at the surface and between 130/230 and 120/220).

Regarding claim 2, Rhodes discloses that the diode electrode structure may be formed with an arsenic implant (paragraph 0026; 0028).

Regarding claim 3, Rhodes discloses that the intervening portion of the first well is a continuous area around the diode electrode structure (see paragraphs 0025-0026; 120 surrounds 115; and 130 is disposed in 115 such that it is spaced away from 120).

Regarding claim 4, Rhodes discloses that the interval between the field oxide and the diode electrode structure is about equal to one depletion region at the operating applied bias (see

paragraph 0043), which indicates that a substantial portion of the depletion region does not extend to the first oxide layer.

Regarding claim 5, Rhodes discloses that the well may be formed in an epitaxial layer (see paragraph 0023).

Regarding claims 6 and 7, Rhodes discloses that the oxide layer is formed using LOCOS or a shallow trench isolation (paragraph 0025).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,281,533 to Miyagawa et al. discloses teachings on the spacing required between a field oxide region and a photodiode doped region to minimize leak currents based on the defects at the edges of the field oxide region.

b. U.S. Patent No. 6,329,233 to Pan et al. discloses a structure substantially similar to that claimed by the Applicant, but wherein the diode is formed directly in a substrate portion, rather than a well.

c. U.S. Patent Publication No. 2004/0033667 to Lee discloses the use of a boron implant to decrease leak currents in a photodiode.

d. U.S. Patent Publication No. 2001/0017367 to Rotstein discloses a method of reducing leak currents in a photodiode by using field isolation materials other than a LOCOS-based field oxide.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd